



CEIUPM

Centro de
Electrónica
Industrial

Digital Embedded Systems @ UPM-CEI

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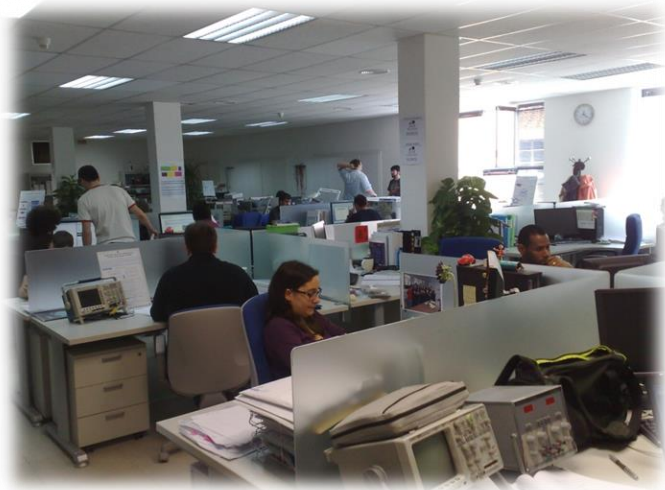


POLITÉCNICA

Centro de Electrónica Industrial (CEI-UPM)



CEIUPM | Centro de
Electrónica
Industrial



Some Numbers

- 46 Full-time researchers
 - 19 Doctors (Faculty, Contracted researchers)
 - 35+ Full-time Students (18 Doctorate, 20 Master)
- 19 Part time, sponsored students (Bachelor)
- 3 Administration & Technicians

Power Electronics

- Power Converters
- Power Supply Architectures
- Modeling & Simulation
- Smart Grids
- Energy Harvesting

Digital Embedded Systems

- Reconfigurable Embedded Systems
- OpenHW and RISC-V
- Internet of Things
- Machine Learning at the Edge
- Post-Quantum Cryptography

Digital Embedded Systems @ UPM-CEI

- 11 professors

- Javier Uceda, Teresa Riesgo*, Yago Torroja, Jorge Portilla, Andrés Otero, Airán Francés, Gabriel Mujica, Jaime Señor, Daniel Vázquez, José Miranda and Alfonso Rodríguez

- 10 full-time PhD students:

- Juan Encinas, Rogelio Hernández, Juan Gallego, Junjiao Sun, Alejandro Redondo, Íñigo Díez de Ulzurrun, Luis Waucquez, Rodrigo Olmos, Juan Granja and Jonathan Valdivieso



<https://github.com/des-cei>

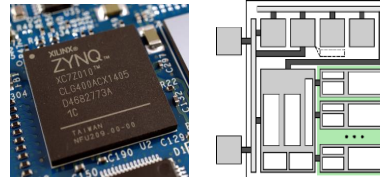
Research Lines

OpenHW and RISC-V



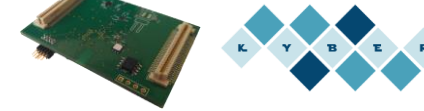
Adaptive RISC-V processors that exploit transparent SW-to-HW computing offloading mechanisms, compiler-assisted automatic code parallelization, and custom domain-specific reconfigurable ISA extensions.

Reconfigurable Hardware and microelectronic design



Developing embedded parallel computing platforms based on HW acceleration and design tools, to obtain energy-efficient, scalable, and run-time adaptive solutions.

Post-Quantum Cryptography



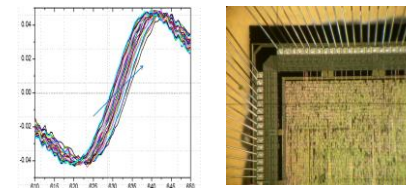
Exploration of different KEM and digital signature schemes for low-end IoT devices in highly dynamic and scalable (1k+ nodes) scenarios.

Internet of Things



Networked embedded systems to face challenges related to the era of smart and sustainable cities, comprising the integration of heterogeneous hardware and software technologies.

Machine Learning at the Edge



Embedded circuits for near-sensor decision making, based on HW/SW embedded signal processing and machine learning techniques

Some of our Research Projects



- Neuromorphic Computing
- RISC-V + CGRA (+ ASIC tapeout)
- Compilers for Heterogenous computing



- Energy Harvesting/micro-power management solutions for Wireless IoT edge device



MYRTUS



- Modelling of reconfigurable Systems
- Resources orchestration in the cloud-edge continuum
- Design of advanced nodes for the edge, based on RISC-V



- RISC-V based wearables
- HW acceleration for Affective Computing
- Custom RISC-V ISA extensions on FPGA

AIRBUS CRISA

Collaboration with Airbus CRISA for the Development of a RISC-V Architecture for Space (Industrial Council of the CEI)

Involvement in “PERTE Chip” Calls

AR2SEC: ARquitecturas de alto rendimiento para SEctores Críticos



SOÑAMOS: Soluciones de diseño y Arquitecturas Microelectrónicas para Salud



Programa Misiones de Ciencia e Innovación

Cátedra PERTE Chip UPM-INDRA en Microelectrónica

- RISC-V for safety-critical applications
- Embedded FPGAs and SiP/chiplets
- Fault-tolerance for aerospace

<https://blogs.upm.es/catedrachip/>

TALENT to Concept (T2C) (Proyectos Prueba de Concepto 2022)

- Silicon implementation of RISC-V + CGRA system
 - Run #1: Baseline architecture
 - Run #2: Low-power version



Dynamic ISA Extensions and IoT Applications

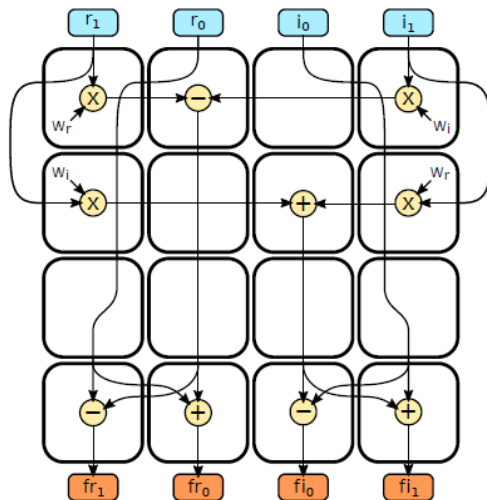
Dynamic ISA Extensions and Reconfigurable Accelerators

FPGA-Based RISC-V Systems

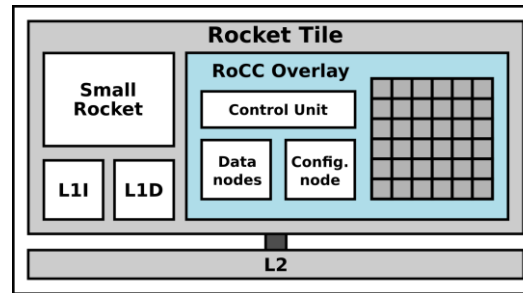
On-Demand Instructions/Datapath
(Load/Unload Extensions at Run Time)

Low-Power Low-Area Processors

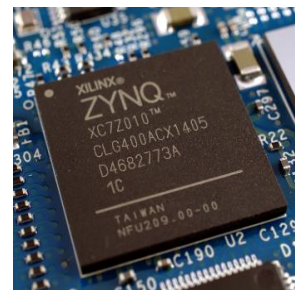
Run-Time Adaptive RISC-V
Processor Datapaths



Memory-Mapped Overlay



<https://github.com/ucb-bar/chipyard>

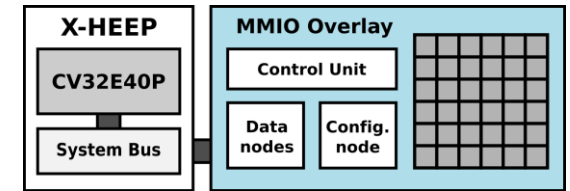


Jornada Ciencia e Industria - AEE



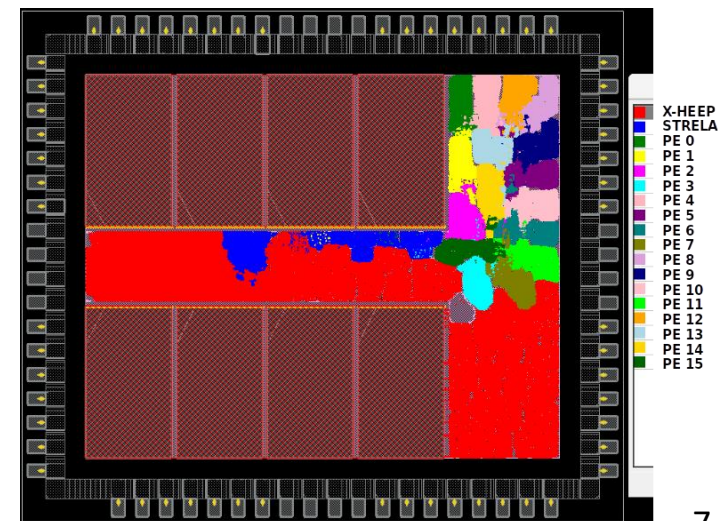
5/02/2025

ISA Extensions Overlay



<https://github.com/esl-epfl/x-heap>

TSMC 65nm LP



Secure & Safe Adaptive RISC-V Processors

Safety

RISC-V Accelerators (Domain-Specific/Custom ISA Extensions)
Spatial/Temporal Redundancy (TMR, Lockstep)
ECCs for Memory Subsystems
RTOS (RTEMS, Zephyr)

Multi-Core Systems
Spatial/Temporal Redundancy (TMR, Lockstep)
Deterministic Communication Infrastructures (Buses)
Workload Balancing and Task Migration

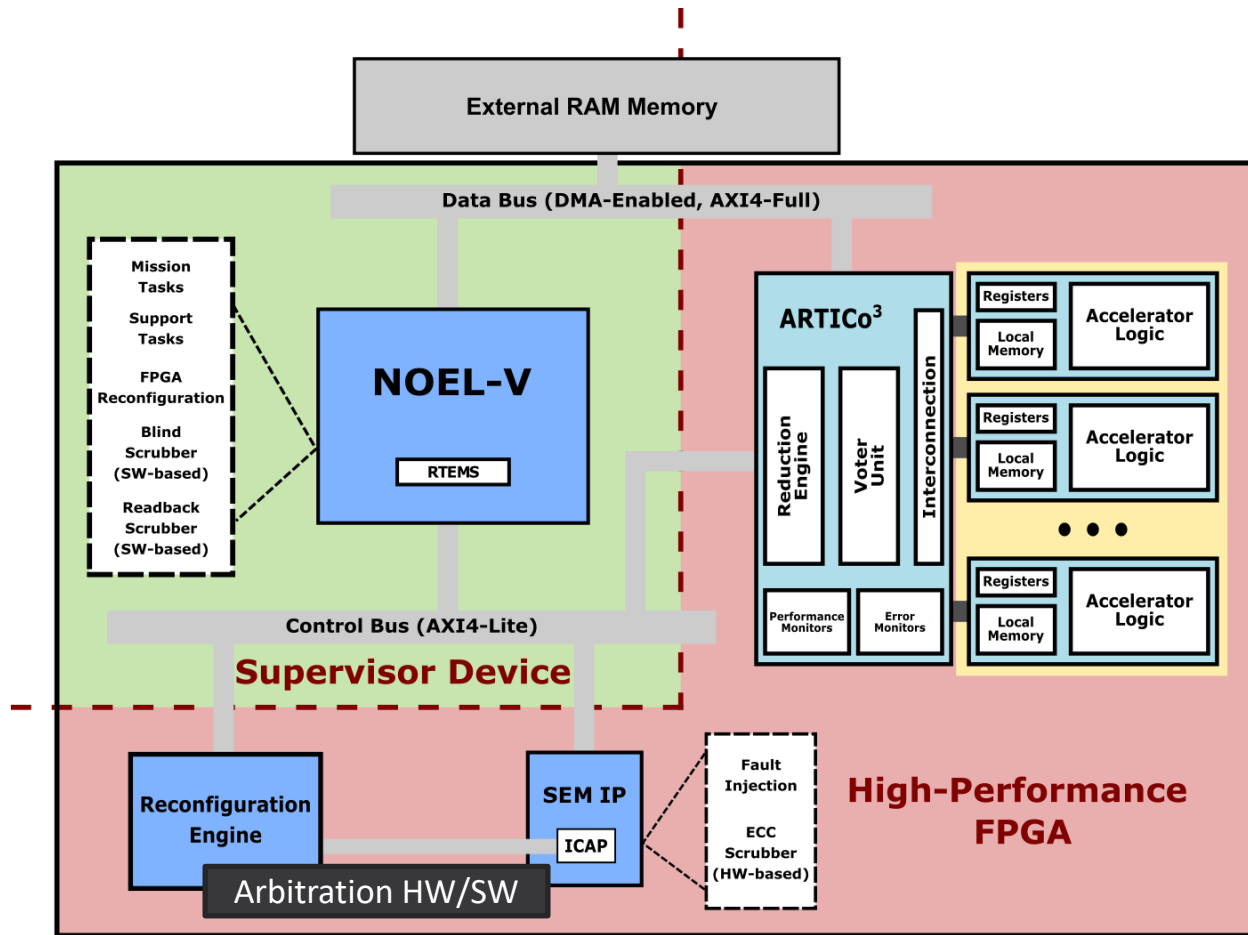


Security

RISC-V Accelerators (Domain-Specific/Custom ISA Extensions)
Lightweight & Post-Quantum Cryptography

RISC-V Accelerators (Standard ISA Extensions)
Scalar/Vector Crypto

Hardening Open-Source MPSoCs for Space Applications



- Migration from ARM Cortex-R5 processors to NOEL-V (RISC-V)
- Implementation on reference NOEL-V design on KC705 (Kintex-7) board **HW**
- Integration of ARTiCo³ on NOEL-V subsystem w/ AHB2AXI bridges **HW**
- Integration of HWICAP on NOEL-V subsystem to support reconfiguration **HW**
- Integration of scrubber and fault injection mechanisms (SEMIP + SW) **HW SW**
- Development of low-level drivers (HWICAP, SEMIP and DMA engine) **SW**



<https://github.com/des-cei/artico3>

...and much more!

- Compilers and Architectures of Adaptive RISC-V Processors
 - MLIR-based C-to-CGRA compilation frameworks
- IPs for Post-Quantum & Lightweight Cryptography
 - CRYSTALS-Kyber, FALCON, ASCON, etc.
- Neuromorphic Computing
 - Optimized SNN accelerators on FPGAs/SoCs
 - Online and on-chip continual learning

**THANK YOU FOR
YOUR ATTENTION**